REMARKS

Claims remaining in the present patent application are Claims 1-8 and 21-52. Claims 1-8 and 21-28 are amended. Claims 29-51 are newly added. No new matter is added. The Applicants respectfully request reconsideration of the above captioned patent application in view of the amendments presented herein and the following remarks.

Request for Examiner Interview

Applicants respectfully request an Examiner Interview in conjunction with the Examiner considering this response.

35 USC § 132(a)

The rejection under 35 USC § 132(a), presented in the Official Action of August 21, 2008, is not presented in the present Official Action. Applicants conclude that the arguments presented in traverse were persuasive and that this rejection has been withdrawn.

35 U.S.C. § 112

The arguments presented in traverse of the previous rejection under 35 U.S.C. § 112 were found persuasive, and this rejection has been withdrawn.

35 U.S.C. § 102

Claims 1-8 and 21-28 stand rejected under 35 U.S.C. § 102(b) as being allegedly unpatentable over Rastegar et al. (US 5,422,591, "Rastegar"). Applicants respectfully assert that embodiments of the present invention as recited in Claims 1-8 and 21-28 are patentable over Rastegar for the following reasons.

With respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "a first input for controlling the switch coupled to a first N-well bias supply line" as recited by Claims 1 and 21.

The rejection alleges "first input B (is) capable of controlling said switch…." Applicants traverse. The rejection's own citation (col. 4, l. 2+) disavows such a configuration: "[w]hen reading a high signal at A, control 30 connects node 20 input at B to the well-tie of transistor Q1 through C." Thus,

the cited art teaches that input B may be switched to output C, as controlled by input A. It is appreciated that in this passage and the whole of Rastegar, input B is not taught to control switch 30, in contrast to such allegation of the rejection.

As understood by Applicants, Rastegar teaches only one signal for controlling switch 30, "input signal N1out," which is connected to input A of control 30. Per Rastegar, "[t]his switching is controlled by input signal N1out" (column 3 lines 61-64). Rastegar fails to teach that input B has any control function for switch 30. In contrast to being a controlling input, Rastegar teaches that the input at B is one possible, e.g., switched, coupling to the output of the switch (output C). For example, "[w]hen reading a high signal at A, control 30 connects node 20 input at B to the well-tie of transistor Q1 through C" (column 4 lines 2-4).

Thus, the alleged "first input B for controlling said switch" does not control the switch as alleged. As taught by Rastegar, input B is incapable of controlling switch 30. For this reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "a first input for controlling the switch coupled to a first N-well bias supply line" as recited by Claims 1 and 21.

The rejection argues that input B is coupled to source/drain of NMOS transistors, and hence meets the limitation of "N-well." Applicants respectfully assert that the limitation further recites "coupled to a first N-well bias supply line." The rejection appears to ignore this portion of the recited limitation. While input B may be coupled to an n-well, Applicants respectfully assert that mere coupling to an n-well is insufficient to suggest the entirety of this recited limitation. As recited, the coupling must be to an "N-well bias supply line."

Rastegar does not teach that input B is an "N-well bias supply line." For example, input B is not coupled to any source, e.g., a power supply, of a bias voltage. Hence, node 20/input B/DQ cannot supply any bias voltage to the n-wells. Moreover, input B does not supply anything to an n-well. Rather, "[t]he common node 20 (input B, also DQ) between transistors Q1 and Q2 provides the output signal DQ of the output driver circuit" (column 3 lines 56-58, emphasis added). Hence the function and configuration of DQ is to be driven by the source/drain n-wells of Q1, Q2, in contrast to supplying anything to such n-

wells. For example, the n-wells at node 20 drive this signal line, rather than being driven or "supplied" by the signal line.

As input B is incapable of supplying anything to the n-wells, it cannot suggest the recited "N-well bias supply line." For this additional reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Further with respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "a second input for controlling the switch coupled to a substrate bias supply line" as recited by Claims 1 and 21.

As previously presented, there is only one control input to switch 30. Hence, Rastegar can neither anticipate nor render obvious the claimed limitations of "a second input for controlling the switch" as recited by Claims 1 and 21.

For this further reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Still further with respect to Claims 1 and 21, the rejection alleges such second input is suggested by input A, and that input A is coupled to a substrate bias supply line through the line emanating from C. Applicants traverse.

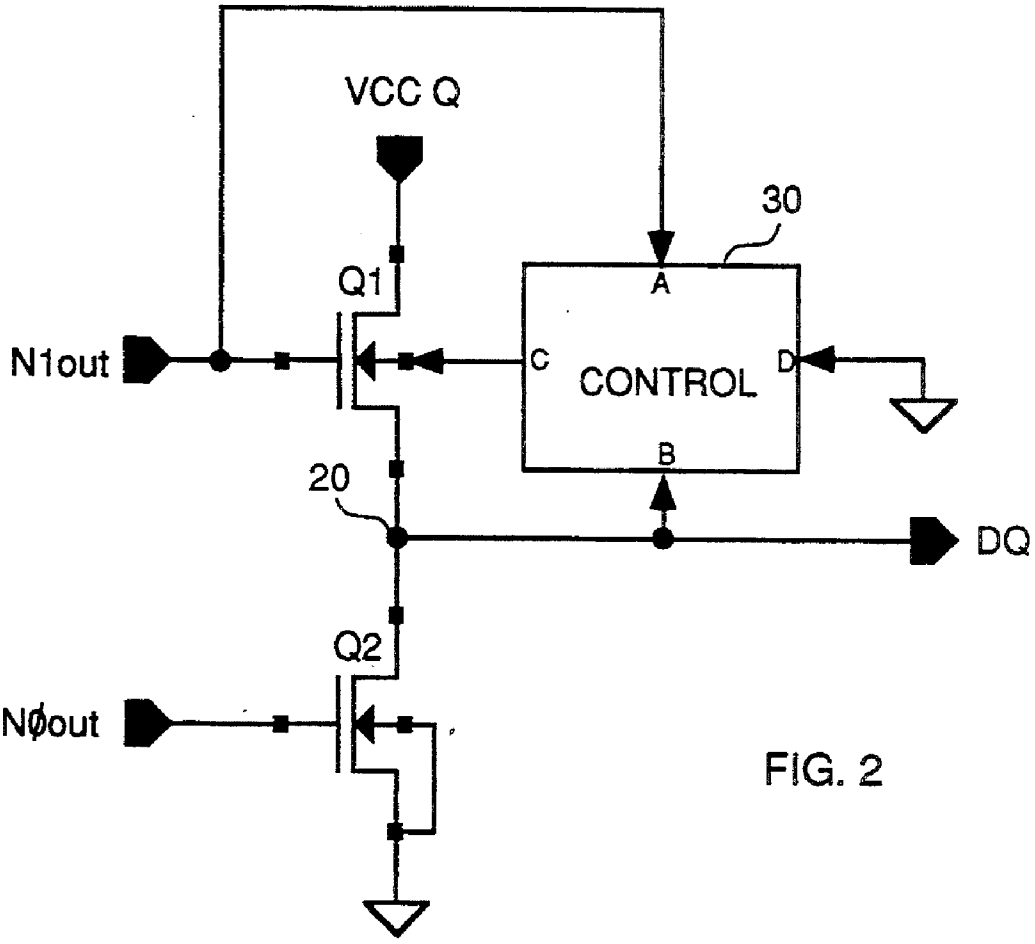

FIG. 2

There is no teaching that A is coupled to C. While both input A (N1 out) and output C touch box 30, Applicants respectfully assert that "touching the same box" fails to provide evidence of coupling. Moreover, signal A is connected to the gate of Q1, whereas signal C is connected to the body of Q1. As is known to those of ordinary skill in the art, the gate of a MOSFET is insulated, e.g.,

separated, from its body by design. The rejection's alleged construction would couple Q1's gate to its body, rendering Q1 inoperative. Applicants respectfully assert that Rastegar does not teach coupling Q1's gate to its body, and that the rejection's interpretation of the art is incorrect.

As input A is not coupled to any transistor body, it cannot be coupled to a "substrate bias supply line" as recited by Claims 1 and 21. For this still further reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Still yet further with respect to Claims 1 and 21, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "wherein the switch is operable to selectively couple the second input to the output terminal responsive to a voltage of the substrate bias supply line" as recited by Claims 1 and 21.

The rejection alleges that switch 30 "is capable, in fact(,) configured, to selectively couple the second input A to the output terminal C responsive to a voltage of the substrate bias supply line." Applicants traverse.

The rejection misinterprets the cited art. In marked contrast to the rejection's allegation, Rastegar teaches that switch 30 selectively couples C to D or B, responsive to A, which is not a substrate bias supply line:

> Control 30 is used for switching the body bias of transistor Q1 (output C) between output node 20 (input B) and ground (input D). This switching is controlled by input signal N1out (input A) (column 3 lines 61-64).

Thus, the control 30 does not function in the manner alleged by the rejection. Rastegar does not teach that input A is coupled to output C. The rejection confuses which signal controls the switch and the nature of the controlling signal ("substrate bias supply line" versus "a signal line connected to a MOSFET gate"). The rejection further confuses which terminals are selectively coupled to the output C.

Consequently, the taught switch 30 is incapable, both structurally and functionally, of being "operable to selectively couple the second input to the output terminal responsive to a voltage of the substrate bias supply line" as recited by Claims 1 and 21.

For this still yet further reason, Applicants respectfully assert that Claims 1 and 21 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 2-8 and 22-28 overcome the rejections of record at least by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 2 and 22, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "the switch is operable to electrically couple the P-type substrate to the ground when a bias voltage is present on the first N-well bias supply line" as recited by Claims 2 and 22.

As previously presented, there is no "N-well bias supply line" taught by Rastegar. Moreover, even assuming, *arguendo*, the rejection's incorrect allegation that the lines connected to node 20, e.g., input B, are a bias supply line, the signals connected to node 20 do not control the switch. Hence, the switch 30 is neither operable to nor configured for coupling anything based on "a bias voltage is present on the first N-well bias supply line" as recited by Claims 2 and 22.

For this additional reason, Applicants respectfully assert that Claims 2 and 22 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 4 and 24, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "further comprising a third input for controlling the switch coupled to a second N-well bias supply line" as recited by Claims 4 and 24.

The rejection does not set forth a structure, or cite to a specific passage of the cited art alleged to suggest the recited "third input for controlling the switch" as recited by Claims 4 and 24. As previously presented, Rastegar teaches only one signal for controlling switch 30. Consequently, Rastegar fails to teach a second signal for controlling the switch, much less the recited "third input for controlling the switch" as recited by Claims 4 and 24.

For this additional reason, Applicants respectfully assert that Claims 4 and 24 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Further with respect to Claims 4 and 24, Applicants respectfully assert that Rastegar fails to teach or suggest the claimed limitations of "a second N-well bias supply line" as recited by Claims 4 and 24. Applicants respectfully assert that Rastegar is silent as to any N-well bias supply lines, much less a second such N-well bias supply line.

The rejection does not set forth a structure, or cite to a specific passage of the cited art alleged to suggest the recited "a second N-well bias supply line" as recited by Claims 4 and 24.

Moreover, even assuming, *arguendo*, the rejection's incorrect allegation that the lines connected to node 20, e.g., input B, represents an N-well bias supply line, there are no similar features in Rastegar. For example, no other n-wells couple to switch 30.

For this further reason, Applicants respectfully assert that Claims 4 and 24 overcome the rejections of record, and respectfully solicit allowance of these Claims.

CONCLUSION

Claims remaining in the present patent application are Claims 1-8 and 21-52. The Applicants respectfully request reconsideration of the above captioned patent application in view of the amendments and remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 504160.

Respectfully submitted,

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